ELECTRO-OPTICAL DEVICE AND METHOD FOR MANUFACTURING THE SAME

Background of the Invention

1. Field of the Invention

The present invention relates to an electric device having a non-light emitting type display such as a liquid crystal display, which an active matrix circuit is formed on a substrate by using thin film transistors (TFTs). In particular, the active matrix circuit of the electric device according to the present invention is drive-controlled by a driving circuit constructed by TFTs formed on the same substrate.

2. Description of the Related Art

Recently, a liquid crystal display is used as a display in an various electric devices of a portable type (for example, a personal computer, a word processor, or an electric pocket note book), by utilizing that the liquid crystal display is thin and light in weight. In particular, since an active matrix type liquid crystal display which controls each pixel one by one using TFTs has superior display characteristic, it is used in many electric devices.

There are various types of an active matrix type liquid crystal displays. One display (first type) has an active matrix circuit formed by using TFTs and its driving circuit constructed by a single crystalline semiconductor integrated circuit chip of an external type. Since it is necessary to connect semiconductor chips and semiconductor packages with a portion around a glass substrate in such unit by using TAB (Tape Automated Bonding) or the like, a display gets relatively large. Also, since a width of wirings (interconnection) extending from the active matrix circuit get small to improve an opening (aperture) rate and the total number of wirings exceeds 1000, there is a technical problem in wiring connection. Further, a large area is required in a connection portion. Furthermore,

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since thermal expansion coefficients between wirings in a glass substrate and wirings in an external chip and thermal expansion coefficients between the wiring in the glass substrate and a tape in a TAB are different from each other, alignment precision is about 60 μm. Therefore, it cannot be applied to a high resolution display which has a pixel pitch of 60 μm or shorter and miniaturization of a display cannot be performed, so that a TFT using an amorphous silicon which can be formed at a low temperature is used in such display.

Another display (second type) has a thin film integrated circuit having an active matrix circuit and driving circuits such as an X-decoder/driver and a Y-decoder/driver which are formed on the same substrate using TFTs. Since an external type semiconductor chip as described above is not used in such display device, a display gets relatively small. Also, since it is not necessary to connect with many wirings, it is superior in miniaturization of a display. In such display, it is necessary to use TFTs constructed by a crystalline silicon having a superior characteristic in a driving circuit.

As a result, the second type display is superior to the first type display in miniaturization of a display. In the second type display, however, further miniaturization, light weighting and thinning are not performed insufficiently. That is, in a personal computer, various semiconductor chips such as a central processing unit (CPU), a main memory, an image signal processing unit, an image memory and the like are formed in a main substrate (main board) other than a liquid crystal display board, and therefore it is necessary to use at least two substrates or boards (main board and liquid crystal display board). To further miniaturization, light weighting and thinning of a display, it is desired to use only one board in stead of two boards.

Summary of the Invention

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The present invention is to perform miniaturization, light weighting and thinning of a display, by arranging semiconductor chips as provided in the above main board in at least one substrate in the a liquid crystal display which a liquid crystal material is held between a pair of substrates. In particular, these chip are provided in a substrate (board) in which an active matrix circuit is formed. Also, a driving circuit for driving the active matrix circuit is formed by using thin film transistors (TFTs).

According to the present invention, there is provided an electric device comprising: a substrate; an active matrix circuit including at least one thin film transistor; a driving circuit including at least another one thin film transistor for driving the active matrix circuit; and at least one semiconductor integrated circuit chip for controlling the driving circuit, wherein the active matrix circuit, the driving circuit and semiconductor integrated circuit chip are formed on the substrate.

Brief Description of the Drawings

Fig.1 is a block diagram showing an electro-optical device;

Fig.2 shows an example of a wire bonding;

Fig.3 shows a schematic view of a liquid crystal display panel according to Embodiments 1 and 2 of the present invention;

Figs.4A and 4B show examples of a FCOG;

Figs.5A to 5G show a process for manufacturing a TFT circuit substrate according to Embodiment 3;

Figs.6A to 6G show a process for manufacturing a TFT circuit substrate according to Embodiment 4;

Figs.7A to 7D show a process for manufacturing a TFT circuit substrate according to Embodiment 5;

Figs.8A to 8I and 9A to 9I show a process for manufacturing a TFT circuit substrate according to Embodiment 6;

Figs.10A to 10C are an upper view, a cross section view and

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a circuit arrangement view of the TFT circuit according to Embodiment 6, respectively; and

Figs.11A to 11E show a process for manufacturing a TFT circuit substrate according to Embodiment 7.

Detailed Description of the Preferred Embodiments

Fig.1 shows concept of the present invention. In Fig.1, an active matrix circuit 14 having a plurality of pixels which each includes a TFT 11, a pixel electrode 12 and an auxiliary capacitor 13 and its driving circuit for driving the active matrix circuit 14 are formed by using TFTs on a substrate (board) 15 made of a glass also used as a liquid crystal display substrate. The driving circuit has an X-decoder/driver 75, a Y-decoder/driver 76 and an X-Y divider 74. The driver circuit may include the X-Y divider 74, or the X-Y divider 74 may be included in a chip as described later.

Another chips are further provided on the substrate 15. these chips are connected with circuits on the substrate 15 by a wire bonding, a chip on glass (COG) including a flip chip on glass (FCOG) method or the like. In Fig.1, a correction memory 71, a memory 73, a CPU (central processing unit) 72 and an input port 70 are used as chips provided by the above method, another chip may be provided.

When the wire bonding is used, a shape having a cross section as shown in Fig.2 is obtained. That is, a chip 22 is mounted by an upward formed terminal portion 23 on a glass substrate 20 in which a circuit is manufactured, and a terminal electrode 21 of the circuit is connected with the terminal portion 23 of the chip 22 by a bonding wire 24 made of a metal. This portion is sealed (covered) by a resin 25 to protect a connection portion from an external shock. In order to stably maintain terminal connection/adhesion, it is desired that a surface of the terminal electrode 21 is a metal such as aluminum. In the wire bonding, since the resin 25 rises largely

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in a terminal connection portion, the resin 25 gets thick.

In the FCOG as shown in Figs.4A and 4B, a chip 42 is mounted by a downward formed terminal portion 43 on a glass substrate 40 in which a circuit is manufactured, and a terminal electrode 41 of the circuit is connected with the downward formed terminal portion 43 of the chip 42 by a bump 44 (Fig.4A) or metal particles 46 (Fig.4B). This portion is sealed by a resin 45 to fix the chip 42 on the substrate 40. As a result, since a thickness of the terminal connection portion substantially corresponds to a thickness of a chip, a thin type display can be manufactured. Also, a material other than aluminum, for example, a transparent conductive oxide film (ITO, Indium tin Oxide or the like) can be used in a terminal on a glass substrate. Commonly, when an active matrix circuit for a liquid crystal display is formed on a glass substrate, since wirings of most upper layer are constructed using the transparent conductive oxide film in many case, the FCOG is superior in this point.

The input port 70 is a circuit for receiving an input signal from an external, for example, a main computer, and converting the received input signal into an image signal. The correction memory 71 is a memory which is inherent in an active matrix panel and is used to correct the input signal or the like in accordance with a characteristic of the active matrix panel. In particular, the correction memory 71 is a non-volatile memory and stores information inherent in each pixel. When a point defect produces in pixels of an electro-optical device, a correction signal is generated with respect to pixels around a pixel which the point defect produces, so that the point defect is compensated. When a pixel is dark in comparison with surround pixels, a signal that the pixel has the same brightness as that of the surround pixels is generated. Since defect information of pixels differs in each of the active matrix panels, information stored in the correction memory 71 differs

in each of the active matrix panels. The CPU 72 and the memory
73 are the same functions as these of the commonly used
computer, and the memory is a RAM (Random access memory) and
stores image information corresponding to each pixel.
[Embodiment 1]

Fig.3 shows a schematic view of a liquid crystal display
panel according to an embodiment of the present invention. In
Fig.3, a substrate (board) 29 is placed opposite to the
substrate (board) 30 and a liquid crystal material is held
between the substrates 29 and 30. An active matrix circuit 31
and peripheral driving circuits 32 to 34 for driving the active
matrix circuit 31 are formed using thin film transistors (TFTs)
on the substrate 30 such as a glass substrate. Also, main
memory chips 36, MPU (microprocessing unit) 37 or CPU (central
processing unit) and correction memories 38 are adhered to a
surface of the substrate 30 in which the above circuits 31 to 34
are formed, and electrically connected with the above circuits
31 to 34. For example, when chips are connected with a
substrate by a FCOG, a wiring terminal portion (wiring
connection pad) 39 (corresponding to a wiring portion 41 of
Figs.4A and 4B) made of the ITO are formed in a portion 35 of
the substrate 30.

In the embodiment, a connection point having a shape as
shown in Figs.4A and 4B is used. In Fig.4A, a conductive
projection (bump) 44 formed in an electrode portion 43 of a chip
42 is electrically connected with a wiring portion 41 on a
substrate 40, and an organic resin 45 is used to fix the chip 42
on the substrate 40. Gold formed by an electroless plating may
be used as the bump 44.

In Fig.4B, the substrate 40 is adhered to the chip 42 by
using an organic resin in which conductive particles (for
example, gold particles) 46 are distributed. Therefore, a
circuit connection is performed by contacting the wiring portion
41 with the conductive particles 46 distributed between the chip

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42 and the electrode portion 43. A light-curable resin, a heat-curable resin, a natural-curable resin or the like is used as the organic resin for adhesive. Injection of a liquid crystal material to a liquid crystal display may be performed after adhering the chip.

After the above processes, a CPU and a memory are formed on a substrate for a liquid crystal display, thereby to construct an electric device such as a personal computer by using one substrate.

[Embodiment 2]

A panel as shown in Fig.3 is manufactured. The active matrix circuit 31 and the peripheral driving circuits 32 to 34 are formed using TFTs on the substrate 30. The main memory chips 36, the MPU (microprocessing unit) 37 or CPU (central processing unit) and the correction memories 38 are adhered to a surface of the substrate 30 in which the above circuits 31 to 34 are formed, and electrically connected with the wiring terminal portion (wiring connection pad) 39 (corresponding to the terminal electrode 21) which is made of an aluminum alloy thin film and formed on the substrate 40 by a wire bonding as shown in Fig.2. A gold fine line is used as a bonding wire.

[Embodiment 3]

In this embodiment, chips are adhered to a TFT circuit (monolithic type active matrix circuit) substrate by a FCOG, to construct further improved circuit. A process for manufacturing a monolithic type active matrix circuit will be described later using Figs.5A to 5G. A silicon oxide film having a thickness of 1000 to 3000 Å is formed as a base oxide film 502 on a substrate (Corning 7059) 501. A method for forming this oxide film may include a sputtering in an atmosphere containing oxygen or a plasma CVD (Chemical Vapor Deposition).

A silicon film having amorphous or crystalline is formed at a thickness of 300 to 1500 Å, preferably 500 to 1000 Å by a plasma CVD or a low pressure CVD (LPCVD). In order to form an

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crystalline silicon film, after forming an amorphous silicon film, a laser or an intense light equivalent to the laser may be irradiated (light annealing), or thermal annealing may be performed at 500 °C or higher for a long time of period. Also, after crystallization by the thermal annealing, light annealing may be performed to improve crystallization. In crystallization by the thermal annealing, an element (catalytic element) for promoting crystallization of silicon, such as nickel, may be added.

The silicon film is etched to form TFT active layers 503 and 504 of a peripheral driving circuit and a TFT active layer 504 of an active matrix circuit, as island-like regions. Further, an silicon oxide having a thickness of 500 to 2000 Å is formed as a gate insulating film 506 in an atmosphere containing oxygen by a sputtering. A method for forming the gate insulating film may include a plasma CVD.

In the present invention, it is desired that a gate insulating film has a sufficiently high withstanding voltage. This is because a high electric field is applied between a gate electrode and a silicon active layer in anodizing process. Therefore, it is preferred that dinitrogen monoxide (N_2O) or oxygens (O_2) and monosilane (SiH_4) is used in a case wherein a gate insulating film is formed by a silicon oxide film obtained by a plasma CVD. (Fig.5A)

An aluminum film (containing scandium of 0.1 to 0.5 weight %) having a thickness of 2000 Å to 5 μm, preferably 2000 to 6000 Å is formed over a substrate by a sputtering and then etched to form gate electrodes (or gate lines) 507 to 510. The gate line 509 is designed to connect with wirings for anodization (not shown). The gate electrodes 507 and 508 of a peripheral logic circuit are electrically insulated from the wirings for anodization. (Fig.5B)

A substrate is placed into an electrolytic solution, and then the gate line 509 and the gate electrode 510 are anodized

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by flowing a current into the wirings for anodization. An anodization condition is described in Japanese Patent Laid Open Number 5-267667. As a result, anodic oxide films 511 and 512 are obtained in upper and side surfaces of the a gate line 509 and the gate electrode 510. A thickness of the anodic oxides depends on a voltage to be applied. In the embodiment, the thickness is 2000 Å.

The anodic oxide obtained by anodizing in almost neutral solution is fine and hard and has a high withstanding voltage. The withstanding voltage equal to and higher than 70 % of a maximum voltage to be applied in anodization. Such anodic oxide is called a barrier type anodic oxide. (Fig.5C)

By ion doping, an impurity is introduced into an island-like silicon film of each TFT using a gate electrode portion (gate electrode and anodic oxide film around the gate electrode) as a mask in a self-alignment. In this doping, after phosphorus is introduced into a whole surface using phosphine (PH_3) as a doping gas, only the island-like region 503 is covered with a photoresist, and boron is introduced into the island-like regions 504 and 505 using diborane (B_2H_6) as a doping gas. The dose is 4×10^{14} to 4×10^{15} atoms/cm^2 in phosphorus and 1×10^{15} to 8×10^{15} atoms/cm^2 in boron. The dose of boron is higher than that of phosphorus. As a result, an N-type region 513 and P-type regions 514 and 515 are formed. (Fig.5D)

A KrF excimer laser (wavelength of 248 nm and pulse width of 20 ns) is irradiated to improve crystallinity of a portion in which crystallinity deteriorates by impurity introduction to the above impurity regions. An energy density of the laser is 200 to 400 mJ/cm^2, preferably 250 to 300 mJ/cm^2. As a result, the N-type and P-type regions are activated. A sheet resistance of these regions is 200 to 800 Ω/square. This process may be performed by thermal annealing within a heat resistance range of a gate electrode.

A silicon oxide film having a thickness of 3000 to 6000 Å is

formed as an interlayer insulator 516 by a plasma CVD. A multilayer of a silicon nitride film (or a silicon oxide film) and a silicon nitride film may be used as the interlayer insulator 516. The interlayer insulator 516 is etched by a wet etching to form contact holes 517 to 519 in the N-type and P-type regions. Simultaneously, a hole 520 is formed in a gate electrode (gate line). Note that since the anodic oxide film 511 operates as a barrier, etching is stopped, so that the gate line remains unetched. (Fig.5E)

Again, a pattern of a contact hole 520 is formed in the contact hole by a photolithography and then etching is performed using an etchant containing chromic acid, for example, a mixing solution of chromic acid (1 to 5 %) and phosphoric acid (or nitric acid, or acetic acid), thereby to form a contact hole 521. (Fig.5F)

A titanium film having a thickness of 2000 to 6000 Å is formed by a sputtering and then etched to form electrode-wirings 522 to 524 of a peripheral circuit, a data line 525 of an active matrix circuit and an electrode 526 of a pixel TFT. The wiring 523 is connected with the gate line 509.

An ITO film having a thickness of 500 to 1500 Å is formed by a sputtering and then etched to form the pixel electrode 527. A silicon nitride film 528 having a thickness of 1000 to 3000 Å is formed as a passivation film. Therefore, peripheral logic circuits and the active matrix circuit are integrated. (Fig.5G)

A silicon nitride film in a terminal portion (corresponding to the portion 41) connecting with an external IC chip is etched to expose an ITO wiring pad of a terminal connection portion. IC chips are adhered by the FCOG as shown in Figs.4A and 4B.

[Embodiment 4]

This embodiment relates to a method for adhering IC chips to a TFT circuit substrate in which a monolithic type active matrix circuit for a liquid crystal display device is formed by the FCOG, as shown in Figs.6A to 6G. In the embodiment, a CMOS

circuit is used as a peripheral circuit. Also, only NTFT is shown as a peripheral circuit TFT, and a peripheral logic circuit is shown in a left side and an active matrix circuit is shown in a right side.

A base silicon oxide film 602 having a thickness of 2000 Å is formed on a glass substrate by a plasma CVD. A raw material gas in the plasma CVD is monosilane (SiH_4) and dinitrogen monoxide (N_2O). A substrate temperature in film formation is 380 to 500 °C, for example, 430°C. The formed silicon oxide film 602 has a relative low etching rate and is solid. This is because since dinitrogen monoxide is used as the raw material gas, a silicon oxide/nitride film containing nitrogen of 1 to 10 % is obtained. A typical etching rate is 800 to 1100 Å/minute using acetic acid-added buffer hydrofluoric acid (ABHF) (hydrofluoric acid : ammonium fluoride : acetic acid = 1 : 50 : 50) at 23 °C.

An amorphous silicon film having a thickness of 500 Å is formed by a plasma CVD. Thermal annealing is performed for 1 hour at 550 °C in an atmosphere containing oxygen, to form an extremely thin (about 40 to 100 Å by estimate) silicon oxide film on a surface of the amorphous silicon film. By a spin coating, an extremely thin film of nickel acetate is formed using a solution of nickel acetate of 1 to 100 ppm. A thin silicon oxide film is formed first on a surface of the amorphous silicon film, in order to distribute a solution on a surface of the amorphous silicon film.

Thermal annealing is performed for 4 hours at 550 °C in an atmosphere containing nitrogen. The nickel acetate is decomposed at about 400 °C, thereby to obtain nickel. Since a thin film of nickel acetate is adhered substantially to the amorphous silicon film, nickel is diffused into the amorphous silicon film by the thermal annealing. Therefore, the amorphous silicon film is crystallized, thereby to form a crystalline silicon region.

A XeCl excimer laser light (wavelength of 308 nm) is irradiated to the silicon film. In the embodiment, an energy density of the laser is 250 to 300 mJ/cm², thereby to further improve crystallinity of the crystalline silicon film. Further, in order to relax stress-strain by a laser irradiation, thermal annealing is performed again for 4 hours at 550 °C.

The silicon film is etched to form island-like active layers 603 and 604. A silicon oxide film 605 having a thickness of 1200 Å is formed as a gate insulating film by a sputtering.

An aluminum (containing scandium of 0.2 to 0.3 weight %) film having a thickness of 4000 Å is formed by a sputtering. By anodizing its surface, an aluminum oxide film (not shown) having a thickness of 100 to 300 Å is formed. Since the aluminum oxide film is present, the aluminum film has high adhesion to a photoresist. Also, by prevent a current leaking from a photoresist, a porous type anodic oxide is effectively formed in sides of a gate electrode or the like in anodization process described below.

A photoresist (for example a product by Tokyo Ohka Co. Ltd, OFPR800/30cp) is formed by a spin coating and then is patterned to form gate electrodes 609 and 611 and a gate line 610. The gate electrode 609 and the gate line 610 in a peripheral circuit are electrically insulated from the gate electrode 611 in an active matrix circuit. Photoresists (masks) 606 to 608 used in etching remain. (Fig.6A)

A porous anodization is performed by flowing a current through the gate line 610, i.e., the gate electrode 611 in a state that the photoresists remain, to form porous anodic oxides 612 and 613 in sides of the gate electrode (gate line). An acid solution such as citric acid, oxalic acid, phosphoric acid, chromic acid or sulfuric acid, of 3 to 20 %, are used in the anodization. A voltage of 10 to 30 V is applied to the gate electrode. In the embodiment, the anodization is performed for 20 to 80 minutes at 10 V in an oxalic solution (pH=0.9 to 1.0 at

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30°C). A thickness of an anodic oxide is controlled by an anodization period of time. By the anodization using an acid solution, the porous anodic oxide is formed. In the embodiment, a thickness of the porous anodic oxide is 3000 to 10000 Å, for example, 5000 Å. (Fig.6B)

After the photoresists are removed, barrier anodization is performed by flowing a current through the gate line 610, to form fine barrier type anodic oxide films 614 and 615 each having a thickness of 1200 Å in side and upper surfaces of the gate line (gate electrode). (Fig.6C)

The silicon oxide film 605 is etched using the porous anodic oxides 612 and 613 as masks by a dry etching, to form gate insulating films 617 and 618. This etching may include a plasma mode of isotropic etching or a reactive ion etching mode of anisotropic etching. Note that it is important not to overetch an active layer by increasing sufficiently a selection ratio of silicon and silicon oxide. For example, when CF_4 is used as an etching gas, an anodic oxide is not etched and only the silicon oxide film 605 is etched. Also, the silicon oxide films 617 and 618 formed under the porous anodic oxides 612 and 613 remain unetched. (Fig.6D)

Only the porous anodic oxides are etched using a mixing solution of phosphoric acid, acetic acid and nitric acid. The barrier anodic oxides 614 and 615 are not almost etched by the mixing solution. Since aluminum is etched by the mixing solution, peripheral circuit portions are masked by using photoresists to protect gate electrodes of the peripheral circuit portions. Therefore, a photolithography process is further added in comparison with Embodiment 3.

By ion doping using the gate insulating film, impurities (phosphorus and boron) are introduced into an active layer. Although only NMOS is shown in figures, boron is also doped. In doing of phosphorus, an accelerating voltage is relatively low (10 to 30 KeV) and a dose is relatively high (5 x 10^{14} to 5 x

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10^{15} atoms/cm^2). Since the accelerating voltage is low, an ion introducing depth is shallow, thereby to introduce the phosphorus into mainly regions 619 and 620 in which a silicon layer is exposed.

Phosphorus is introduced with a relatively low dose of 1 x 10^{12} to 1 x 10^{14} atoms/cm^2 at a relatively high accelerating voltage of 60 to 95 KeV. Since the accelerating voltage is high, an ion introducing depth is deep, thereby to introduce the phosphorus into a region 621 covered with a gate insulating film. As a result, the regions 619 and 620 into which the phosphorus having a high concentration is doped and the region 621 into which the phosphorus having a low concentration is doped are formed. That is, with respect to a pixel TFT, so called double drain structure can be obtained. In boron, the same process may be performed.

Thermal annealing is performed for 1 hour at 450 °C, to activate the doped impurities. In the embodiment, since nickel is used as a promoting element for crystallization, activation can be performed at low temperature than that in normal activation. (Fig.6E)

A multilayer film 622 having a silicon oxide film (200 Å in thickness) and a silicon nitride film (4000 Å in thickness) is deposited (formed) as a first interlayer insulator by a plasma CVD, and then etched by a dry etching, to form contact holes 623 to 627. (Fig.6F)

A three layer metal film having titanium (500 Å in thickness), aluminum (4000 Å in thickness) and titanium (500 Å in thickness) is deposited by a sputtering and then etched to form electrode-wirings 628 to 631. Further, by a plasma CVD, a silicon oxide film 632 having a thickness of 2000 Å is deposited as a second interlayer insulator and a contact hole is formed in a drain electrode 631 of a pixel TFT, to form a pixel electrode 633 by an ITO. Therefore, a monolithic type active matrix circuit can be manufactured. (Fig.6G)

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In the above processed substrate, IC chips are mounted on ITO wiring pads of the terminal portion (corresponding to the portion 41) which is connected with external IC chips and adhered by the FCOG as shown in Figs.4A and 4B.

[Embodiment 5]

In the embodiment, chips are adhered to a TFT circuit (monolithic type active matrix circuit) substrate by a wire bonding, to construct further improved circuit. Figs.7A to 7D show a process for fabricating an active matrix circuit according to the embodiment of the present invention. In Figs. 7A to 7D, a left side is a peripheral logic circuit region, and a right side is an active matrix circuit region.

By a sputtering, a base oxide film 701 having a thickness of 2000 Å is deposited on a glass substrate (not shown). Also, an ITO film having a thickness of 500 Å is formed on the base oxide film 701 by a sputtering and then etched to form wirings 702 to 704 of the peripheral logic circuit region and a wiring 705 and a pixel electrode 706 of the active matrix circuit region.

An amorphous silicon film having a thickness of 500 to 1500 Å is deposited by a plasma CVD or a LPCVD with monosilane or disilane as a raw material gas. It is preferred that an oxygen concentration in the amorphous silicon film is 10^{18} atoms/cm^3 or less.

Phosphine and boron are doped by ion doping similar to that in a known CMOS manufacture. That is, phosphorus is doped, a region forming an N-channel type TFT is masked by photoresists, and then boron is doped into a region forming a P-channel type TFT.

A doping gas for doping phosphorus is phosphine (PH$_3$) and a doping gas for doping boron is dibolane (B$_2$H$_6$). It is preferred that an accelerating voltage is 5 to 30 kV in phosphorus and boron. A dose is 1 x 10^{14} to 5 x 10^{15} atoms/cm^2, for example, 2 x 10^{14} atoms/cm^2 in phosphorus and 5 x 10^{14} atoms/cm^2 in boron.

A portion (between a source and a drain) as a channel

forming region of each TFT is etched to form N-type semiconductor regions 707, 708, 711 and 712 and P-type semiconductor regions 709 and 710. A substantially intrinsic amorphous silicon hydride film 713 having a thickness of 100 to 500 Å, for example, 200 Å, is formed on these regions by a plasma CVD.

In Fig.7A, a KrF excimer laser light (wavelength of 248nm and pulse width of 20 ns) is irradiated using a nonadhesive mask 714 which is not in contact with the film 713, to crystallize the peripheral circuit region (left side) in the film 713. An energy density of the laser is 200 to 400 mJ/cm2, preferably 250 to 300mJ/cm2. Since the irradiated laser light does not reach a region (including the active matrix circuit region) covered with the mask 714, the region remains as the amorphous silicon. Also, regions to which the laser is irradiated are crystallized in not only the film 713 but also the regions 707 to 710.

The silicon films (N-type and P-type semiconductor regions and the intrinsic silicon film) are etched at an island shape, to form island-like regions 721 to 723 of a peripheral circuit. Simultaneously, a source 715 and a drain 716 in an N-channel type TFT of a peripheral logic circuit, a source 718 and a drain 717 in a P-channel type TFT of the peripheral logic circuit, and a source 719 and a drain 720 in an N-channel type TFT of an active matrix circuit are also formed. (Fig.7B)

A silicon oxide film 724 having a thickness of 1200 Å is deposited by a plasma CVD using dinitrogen monoxide (N_2O) and oxygens (O_2) as raw materials. Since the film 724 operates as a gate insulating film or a dielectric substance of a retaining capacitor, it is necessary for the film to have a sufficiently low interface level density and a high withstanding voltage. In the embodiment, monosilane and dinitrogen monoxide are introduced into a reaction chamber at 10 SCCM and 100 SCCM, respectively. A substrate temperature is 430 °C, a reaction pressure is 0.3 Torr, and an applied power is 250 W at 13.56

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MHz. These conditions depends on a reaction apparatus to be used.

A film forming speed of the silicon oxide film formed in the above conditions is about 1000 Å/minute. When a mixing solution (at 20 °C) of hydrofluoric acid, acetic acid and ammonium fluoride at a rate of 1 : 50 : 50, respectively, is used, an etching speed is about 1000 Å/minute. A titanium film having a thickness of 2000 to 8000 Å, for example, 3000 Å is deposited by a sputtering and then etched to form gate electrodes 725 to 727 and a retaining capacitor electrode 728.

By a plasma CVD, a silicon nitride film 729 having a thickness of 3000 Å is formed as a passivation film. Therefore, N-channel type and P-channel type TFTs (peripheral p-Si N-ch TFT and peripheral p-Si P-ch TFT) of a crystalline silicon of a peripheral logic circuit, an N-channel type amorphous silicon TFT (pixel a-Si N-ch TFT) of an active matrix circuit and a retaining capacitor can be formed. (Fig.7C)

A TFT structure of the peripheral logic circuit may be different from that of the active matrix circuit. For example, an offset structure as shown in Fig.7D in which the gate electrode of the TFT of the active matrix circuit is formed apart from the drain by a distance x, an off current can be further reduced.

In order to perform the same high speed operation as that of a peripheral logic circuit, it is required that a semiconductor has crystallization, a source and a drain also have crystallization and a sheet resistance is low. In the embodiment, although a laser is irradiated to manufacture a peripheral logic circuit, since not only a channel forming region but also a portion corresponding to a source and a drain are crystallized, the above requirement is satisfied. In order to further improve crystallization of the source and the drain, a catalysis element for promoting crystallization of amorphous silicon, such as nickel, platinum, palladium, cobalt or iron,

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may be added into a silicon film at a concentration of 1×10^{17} to 2×10^{19} atoms/cm^3.

In the above processed substrate, a silicon nitride film 729 of a terminal portion (corresponding to the portion 21) which is connected with an external IC chip is etched to expose titanium wiring-pads of a terminal connection portion, and connected with the IC chip by a wire bonding as shown in Fig.2.

[Embodiment 6]

Figs.8A to 8I show cross sections of an active matrix circuit portion, and Figs.9A to 9I show cross sections of a peripheral circuit portion. Also, Fig.10A is an upper view of a manufactured active matrix circuit, and Figs.8I and 9I represent a cross section of a line A-B-C in Fig.10A. Fig.10B represents a cross section of a line a-b in Fig.10A. Fig.10C shows a circuit arrangement of a active matrix circuit to be manufactured by the embodiment.

First gate wiring-electrodes 802 to 805 are formed on an insulating surface 801 of a glass substrate on which a silicon nitride film (not shown) having a thickness of 1000 Å is formed. The gate wiring-electrodes are formed by etching a polycrystalline silicon film in which a resistance is reduced by phosphorus doping and has 3000 Å in thickness. The polycrystalline silicon film is formed by a low pressure CVD, and has a polycrystalline state at forming this film.

In order to obtain the polycrystalline silicon film , there is the following method other than the above method. That is, after an intrinsic amorphous silicon film is formed by a plasma CVD or a low pressure CVD, an impurity such as phosphorus is introduced into the silicon film by ion doping or the like. Further, thermal annealing is performed at 500 to 600 °C. In the thermal annealing, an element for promoting crystallization, such as nickel may be added slightly. In the embodiment, silicon is used. However, silisides of various metals may be used.

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By a plasma CVD, a silicon nitride film 806 having a thickness of 3000 to 6000 Å, for example, 4000 Å, is deposited and operates also as a gate insulating film. Also, an amorphous silicon film having a thickness of 300 to 1000 Å, for example, 500 Å, is formed by a plasma CVD and then etched to form island-like regions 807 to 809. (Figs.8A and 9A)

By a plasma CVD, a silicon nitride film 810 having a thickness of 3000 to 6000 Å, for example, 2000 Å is deposited and operates also as a gate insulating film. A laser light is irradiated into only a peripheral circuit portion to crystallize the island-like silicon film. The laser is a XeCl excimer laser (wavelength of 308 nm). An irradiation energy density of the laser and the number of pulse are changed in accordance with film characteristics of the silicon film and the silicon nitride film 810.

The silicon nitride films 806 and 810 are etched to from a contact hole (not shown) which reaches the first gate wiring. This contact hole is used to form a contact between the first gate wiring and a second gate wiring which is formed on the first gate wiring and corresponds to a contact 845 as shown in Figs.10A and 10B.

After forming the contact hole, an aluminum film 811 having a thickness of 3000 to 8000 Å, for example, 5000 Å, is formed by a sputtering. When the aluminum film 811 contains scandium (Sc) of 0.1 to 0.5 weight %, generation of hillock can be prevented. (Figs.8B and 9B)

The aluminum film 811 is etched to form second gate wiring-electrodes 812 to 815. As a result, a contact of the first gate wiring and the second gate wiring is formed through the formed contact hole. It is necessary to completely cover the contact hole with the second gate wiring. This is because when the first gate wiring constructed by silicon is exposed in a contact hole, a current flows through an exposed portion in an anodizing process, thereby not to progress an anodizing reaction. (Figs.8C

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and 9C)

In an electrolytic solution, a current is supplied to a gate electrode. An ethylene glycol solution which is obtained by adding ammonia to tartaric acid of 3 to 10 % and has 6.8 to 7.2 pH is used. When the solution has about 10 °C lower than a room temperature, an oxide film having high quality is formed. Therefore, barrier anodic oxides 816 to 819 are formed in an upper and side surface of the second gate wiring-electrodes. A thickness of the anodic oxide is proportional to an applied voltage and is preferably 1000 to 3000 Å. The anodic oxide having a thickness of 2000 Å is formed at 150 V. In order to obtain an anodic oxide having a thickness of 3000 Å or more, it is necessary to apply 250 V or higher. However, this influences a TFT characteristic. (Figs.8D and 9D)

By dry etching, the silicon nitride film 810 is etched in self-alignment. However, since the anodic oxides are not etched, gate insulating films 820 to 823 remain between gate wiring-electrodes and an island-like silicon layer. (Figs.8E and 9E)

By ion doping, N-type and P-type impurities are introduced into the island-like silicon layers 807 to 809 using gate electrode portions (gate electrode and anodic oxide film around the gate electrode) in self-alignment, to form an N-type impurity regions (source/drain regions) 824 to 827 and a P-type impurity regions 828 and 829. A doping gas in an N-type impurity doping is phosphine (PH_3) and a doping gas in a P-type impurity doping is diborane (B_2H_6). A dose is 5 x 10^{14} to 5 x 10^{15} atoms/cm^2, and an accelerating energy is 10 to 30 keV. A KrF excimer laser (wavelength of 248 nm and pulse width of 20 ns) is irradiated to activate impurity ions introduced into an active layer. (Figs.8F and 9F)

A metal such as a titanium film 830 having a thickness of 50 to 500 Å, is formed on a whole surface by a sputtering method. (Figs.8G and 9G)

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By thermal annealing at 450 to 500 °C, for example, 500 °C for 10 to 60 minutes, titanium reacts with silicon, to form siliside (titanium silicide) regions 831 to 836. In this thermal annealing, the doped impurities are further activated. In stead of thermal annealing for siliside process, laser annealing by a laser light irradiation, and lamp annealing by visible light irradiation or near infrared light irradiation may be performed.

A titanium film is etched using an etching solution obtained by mixing among hydrogen peroxide, ammonia and water at a ratio of 5 : 2 : 2, respectively. since a titanium film (for example, a titanium film which is formed on the silicon nitride film 806 and the anodic oxide film) which is not in contact with the exposed active layer remains in a metal state, it can be etched in this etching process. On the other hand, the titanium siliside is not etched and therefore remains (Figs.8H and 9H)

By a CVD, a silicon oxide film having a thickness of 5000 Å is formed as a first interlayer insulator 837 on a whole surface. Contact holes are formed in a source and a drain in a TFT. After forming the first interlayer insulator, annealing is performed at 400 °C for 10 to 30 minutes. Aluminum wiring-electrodes 838 to 841 are formed and a pixel electrode 842 is formed using an ITO film.

In order not to enter water component, an active ion or the like into a TFT form an external, a silicon nitride film 843 having a thickness of 2000 to 5000 Å, for example, 3000 Å is formed by a plasma CVD, and a pixel portion 844 and a terminal portion (not shown) connecting a peripheral circuit with an external IC chip is opened to expose the ITO film. (Figs.8I and 9I)

By the above processes, a wiring intersection portion 847 in an active matrix circuit, a TFT 848 connected to a pixel, and an N-channel type TFT 849 and a P-channel type TFT 850 in a peripheral circuit is formed to obtain a monolithic type active

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matrix circuit.

Fig.10A is an upper views of a TFT provided with a pixel portion. It is appeared that a gate line extended from a scan driver is a single line in Fig.10A. However, the first gate line 802 is formed in parallel under the second gate line 812. The first and second gate lines are connected with each other through the contact 845. In an active matrix circuit according to the embodiment, one contact is formed for one TFT.

Although one of the first and second gate lines is broken, the whole line does not become inferior. In the embodiment, as shown in Fig.10A, a contact is formed in a branch portion in which the gate lines are branched. This is because, in providing a pad region (wiring region having thick width) for forming a contact, it is not necessary for the branch portion to provide a special space and therefore it is superior in layout.

Fig.10B shows a cross section structure in a line a-b along a gate line as shown in Fig.10A. Figs.10C shows an active matrix circuit having a plurality of circuits each shown in Fig.10A. In Fig.10A, the gate line 812 (and 802) is also branched to a wiring 846 extended under an upper line pixel electrode. A capacitor is formed between the wiring 846 and a pixel electrode and arranged in parallel to a capacitor of a liquid crystal formed by a pixel electrode on a circuit. In the processed substrate, an IC chip is mounted on a terminal portion (corresponding to a portion 41) of an ITO for connecting with an external IC chip and adhered to the IC chip by the FCOG method as shown in Figs.4A and 4B.

[Embodiment 7]

In the embodiment, an IC chip is connected with a monolithic type active matrix circuit (TFT circuit) substrate which an active matrix circuit using amorphous silicon (a-Si) TFTs and a peripheral circuit using crystalline silicon TFTs are formed on the same glass substrate.

Figs.11A to 11E shows a process for manufacturing an

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monolithic type active matrix circuit of the embodiment. A silicon oxide film having a thickness of 1000 to 3000 Å is formed as a base oxide film 902 on a glass substrate 901. By a plasma CVD or a LPCVD, a silicon film 903 having amorphous is deposited at a thickness of 300 to 1500 Å, for example, 500 Å. Further, a silicon oxide film (or a silicon nitride film) having a thickness of 50 to 1000 Å, for example, 200 Å is formed as a protective film 904 by a plasma CVD.

A KrF excimer laser (wavelength of 248 nm and pulse width of 20 ns) is irradiated to improve crystallinity of the silicon film 903. An energy density of the laser is 200 to 400 mJ/cm^2, preferably 250 to 300 mJ/cm^2. (Fig.11A)

The protective film 904 is removed to expose the silicon film 903 and patterned in an island shape to form an N-channel type TFT region 905 and a P-channel type TFT region 906. Further, a gate insulating film 907 is formed by a sputtering in an atmosphere containing oxygen or by decomposing and depositing a TEOS using a plasma CVD.

An aluminum film having a thickness of 2000 Å to 5 μm is formed by a sputtering and then etched to form gate electrodes 908 and 909. Simultaneously, a gate electrode 910 of a reversed stagger type TFT of an active matrix portion is also formed. (Fig.11B)

The substrate is immersed in an electrolytic solution to supply a current to a gate electrode, thereby to form anodic oxide layers 911 to 913 around the gate electrode. It is desired that anodic oxide films of a TFT (left side) of a peripheral circuit region is thin to improve mobility of the TFT and anodic oxide films of a TFT (reverse stagger type TFT in right side) of an active matrix circuit is thick to prevent a gate leakage. In the embodiment, Both anodic oxide films have 2000 to 2500 Å in thickness. (Fig.11C)

By ion doping, an impurity is introduced into an island-like silicon film of each TFT using a gate electrode portion (gate

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electrode and anodic oxide film around the gate electrode) as a mask in self-alignment. That is, phosphorus is introduced first into a whole surface using phosphine (PH_3) as a doping gas. After that only the island-like region 905 is masked by a photoresist, and then boron is introduced into only the island-like region 906. A dose is 2×10^{15} to 8×10^{15} atoms/cm^2 in phosphorus and 4×10^{15} to 10×10^{15} atoms/cm^2 in boron. The dose of boron is higher than that of phosphorus.

A KrF excimer laser (wavelength of 248nm and pulse width of 20 ns) is irradiated to improve crystallinity of a portion in which crystallinity deteriorates by introduction of the impurity. An energy density of the laser is 200 to 400 mJ/cm^2, preferably 250 to 300mJ/cm^2. (Fig.11D)

As a result, N-type regions 914 and 915 and P-type regions 916 and 917 are formed. A sheet resistance of these regions is 200 to 800 Ω/square.

By a plasma CVD, a silicon nitride film having a thickness of 3000 Å is formed as an interlayer insulator 918 on a whole surface. The silicon nitride film is an interlayer insulator in a peripheral circuit. However, since the silicon nitride film operates as an gate electrode of a TFT in an active matrix circuit, it is necessary to pay attention to its film manufacture.

An amorphous silicon layer 919 having a thickness of 100 to 500 Å, for example, 200 Å, is formed on the gate electrode 910 of an active matrix portion, and then a source 920 and a drain 921 of an amorphous silicon TFT is formed using a microcrystalline silicon layer (500 to 1000 Å in thickness) formed by a plasma CVD. A pixel electrode 925 is formed using a transparent conductive material such as an ITO in a TFT of an active matrix portion.

Contact holes are formed in a source and a drain of each TFT of a peripheral circuit portion, to form aluminum wirings 922 to 924. An invertor circuit is manufactured using an N-channel

type TFT and a P-channel type TFT in left side. Annealing is performed for 2 hours at 350 °C in an atmosphere containing hydrogen, to decrease dangling bonds of a silicon film. By the above processes, a peripheral circuit and an active matrix circuit are integrated.

In the embodiment, a reversed stagger type TFT is used as an amorphous silicon TFT of an active matrix circuit, so as not to irradiate light into a channel portion. This is because conductivity of an amorphous silicon changes by light irradiation. In the processed substrate, an IC chip is connected with a terminal portion (corresponding to the portion 21) of an aluminum wiring connecting with an external IC chip by using the wire bonding method as shown in Fig.2.